REMARKS

Claims 1-26 were pending. Claims 6, 14, and 24 have been canceled. Claims 1, 4, 11, 15, 19, 22 and 24 have been amended. Accordingly, claims 1-5, 7-13, 15-23, and 25-26 remain pending subsequent entry of the present amendment.

In the present Office Action, claims 1-9, 11-17 & 19-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,801,208 ("Keshava"), in view of U.S. Patent No. 6,819,321 ("Hsieh"), and in further view of U.S. Patent No. 6,825,848 ("Fu"). In addition, claims 10, 18 & 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Keshava, in view of Hsieh, and in further view of Fu, and still in further view of U.S. Patent No. 6,681,297 ("Chauvel"). Applicant respectfully traverses at least some of the above rejections and requests reconsideration in view of the following discussion.

Generally speaking, each of the independent claims have been amended to incorporate features of a now canceled dependent claims. For example, claim 1 has been amended to incorporate features of prior claims 4 and 6. Applicant believes pending claim 1 to be patentably distinguished from the cited art. Claim 1 now further recites an apparatus

"wherein the graphics unit is configured to:
partition images to be rendered into a plurality of subset areas;
track the number of times data corresponding to each of the subset areas is considered during the rendering of a first image; and
determine for each of the subset areas whether data corresponding to a subset area is cacheable;

wherein the graphics unit includes a plurality of entries, each entry corresponding to one of the subset areas and including an indicator which indicates whether the corresponding subset area is cacheable in the shared cache;

wherein during the rendering of a second image, the graphics unit is further configured to store data evicted from the graphics unit cache in the shared cache only if an indicator in an entry which corresponds to the data

> evicted from the graphics unit cache indicates the data evicted from the graphics unit cache is cacheable in the shared cache, said indicator being set prior to initiating the rendering of the second image.

From the above it is seen that the graphics unit maintains an entry for each of the subset areas of the partitioned image. Each of these entries includes an indicator which indicates whether the corresponding subset area is cacheable. During the rendering of a second image, data evicted from the graphics unit cache may only be stored in the shared cache if the entry corresponding to that particular subset area includes an indicator which indicates the evicted data may be stored in the shared cache. As can be seen, the indicators are particular to subset areas of a partitioned image.

In the present Office Action, Keshava is generally cited as disclosing the features of prior claim 6. However, Keshava discloses an indicator which is used to generally indicate whether or not an L2 cache may be shared by a graphics unit. For example, Keshava discloses:

> "In some embodiments, the graphics engine may include a texture processing unit and a color and depth (C/Z or Color/Z) processing unit. In this embodiment, allocation of portions of the L2 cache may be made to either or both of these processing units. For example, in one embodiment, the driver may allocate the L2 cache according to four modes. In one mode, a non-shared mode, the entire L2 cache is allocated to the processor core. In an equally shared mode, the driver may allocate the L2 cache such that the processor core may access half of the L2 cache and the color/depth processing unit and the texture processing each access an equal portion of the L2 cache, namely, a quarter of the L2 cache is allocated to each processing unit. In a third mode, the C/Z only shard mode, one quarter of the L2 cache is allocated to the color/depth processing unit of the graphics engine while three quarters of the L2 cache is allocated to the processor core. In a fourth mode, the texture only shared mode, one quarter of the L2 cache is allocated to the texture processing unit of the graphics engine while three quarters of the L2 cache is allocated to the processor core." (Keshava, col. 5, lines 28-51).
>
> "Referring again to FIG. 2A, at some point, the driver determines that L2 sharing is no longer needed, as shown in block 92. That is, the

> driver determines that the graphics engine and/or the graphics application no longer needs or will no longer benefit from sharing the L2 cache, or that the processor core needs the L2 cache memory. As above, the driver then writes allocation information in a machine specific register and provides an instruction to the processor which causes the processor to execute an instruction that examines the cache allocation information, as shown in blocks 62 and 64. However, in this situation, the driver instructs the processor to write cache allocation information that includes the allocation action bit set to "release" to the MSR. When a check is made to determine whether to allocate the L2 cache to or release the L2 cache from the graphics engine, as shown in block 66, the processor finds the allocation action bit of the cache allocation information set to "release." Referring again to FIG. 2B, the driver then checks that the L2 cache is currently in shared mode, as shown in block 80. If the L2 cache is in shared mode, the portion of the cache to be returned to the processor core is flushed, as shown in block 82. This ensures that any changes made to data in the L2 cache being used by the graphics engine are not lost and are stored to either the cache memory, the main memory, and/or to disk. The clock speed of the shared portion of the L2 cache is then changed to match the clock speed of the processor core, as shown in block 84. The driver then transitions the graphics engine out of L2 sharing mode and sets the processor core lock bit to unlocked, as shown in block 86. This causes the processor core to begin accessing the entire L2 cache." (Keshava, col. 6, line 47 – col. 7, line 10).

From the above it is seen the Keshava discloses a mechanism whereby various portions of the L2 cache may be allocated for use by the processor and/or graphics unit. If at some point in time sharing is to be discontinued, the portion of the cache to be returned to the processor is flushed to avoid losing changes. Thus, Keshava discloses a general sharing mechanism which is not specific to any data in particular, and clearly not specific to a particular subset area of a partitioned image. Accordingly, Keshava does not disclose the features of the claim wherein separate entries are maintained for each of the subset areas of a partitioned image and an indicator in the entry indicates whether data for that particular subset area is cacheable in the shared cache when being evicted. In view of the above, Applicant submits claim 1 is patentably distinguished. Further, as each of independent claims 11 and 19 include similar features, each of claims 11 and 19 are believed patentable for similar reasons. Likewise, each of the dependent claims are believed patentable for at least the above reasons.

Applicant believes the application is in condition for allowance. However, should the examiner believe issues remain which would prevent the application from proceeding to allowance, the below signed representative would appreciate a phone interview at (512) 853-886 in order to facilitate a more rapid resolution.

CONCLUSION

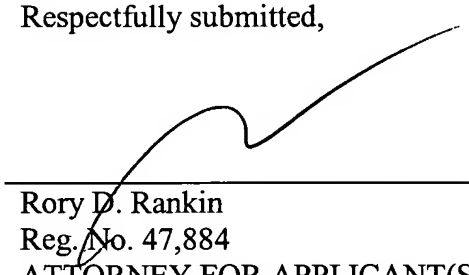
Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-98000/RDR.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

Respectfully submitted,



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Date: September 15, 2005